

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Original) A method to reduce switching noise on an integrated circuit device,
2 said method comprising:
3 providing an integrated circuit device comprising an upper voltage node, a
4 ground, and a plurality of switchable capacitors wherein each said switchable capacitor
5 is connected from said upper voltage node to said ground;
6 tracking an operating mode of said integrated circuit device;
7 selecting an optimal capacitance value based on said operating mode; and
8 selecting a set of said switchable capacitors from said plurality of switchable
9 capacitors to thereby connect said optimal capacitance value from said upper voltage
10 node to said ground.

1 2. (Original) The method according to Claim 1 wherein said step of selecting an
2 optimal capacitance value based on said operating mode is by a method further
3 comprising:
4 determining a proportion of total circuits in said integrated circuit device that are
5 switching in said operating mode; and
6 calculating said optimal capacitance value based on said proportion.

1 3. (Original) The method according to Claim 2 wherein said optimal capacitance
2 value is calculated using a formula based on capacitance loading in switching circuits
3 and capacitance loading in non-switching circuits.

1 4. (Original) The method according to Claim 1 wherein said operating mode
2 comprises a power-saving mode.

1 5. (Original) The method according to Claim 1 wherein said switchable
2 capacitors each comprise a capacitor and a switch connected in series.

1 6. (Original) The method according to Claim 5 wherein said capacitor comprises
2 an MOS device.

1 7. (Original) The method according to Claim 5 wherein said capacitor is
2 connected to said upper voltage node and said switch is connected to said ground.

1 8. (Original) The method according to Claim 5 wherein said capacitor is
2 connected to said ground and said switch is connected to said upper voltage node.

1 9. (Original) The method according to Claim 5 wherein said switch comprises an
2 MOS transistor.

1 10. (Original) The method according to Claim 1 wherein said switchable
2 capacitors each comprise:
3 a PMOS transistor having source, drain, and gate terminals wherein said source
4 terminal is coupled to said upper voltage node;
5 an NMOS transistor having source, drain, and gate terminals wherein said
6 source terminal is coupled to said ground, wherein said drain terminal is coupled to said
7 PMOS transistor gate terminal, and wherein said gate terminal is coupled to said PMOS
8 transistor drain terminal;
9 a first switch coupled between said PMOS transistor gate terminal and said
10 upper voltage node; and
11 a second switch coupled between said NMOS transistor gate terminal and said
12 ground.

1 11. (Original). The method according to Claim 10 wherein said first and second
2 switches comprise MOS transistors.

1 12. (Original) A method to reduce switching noise on an integrated circuit device,
2 said method comprising:
3 providing an integrated circuit device comprising an upper voltage node, a
4 ground, and a plurality of switchable capacitors wherein each said switchable capacitor
5 is connected from said upper voltage node to said ground and wherein said switchable
6 capacitors each comprise a capacitor and a switch connected in series;
7 tracking the operating mode of said integrated circuit device;
8 selecting an optimal capacitance value based on said operating mode by a
9 method comprising:
10 determining a proportion of total circuits in said integrated circuit device that are
11 switching in said operating mode; and
12 calculating said optimal capacitance value based on said proportion; and
13 selecting a set of said switchable capacitors from said plurality of switchable
14 capacitors to thereby connect said optimal capacitance value from said upper voltage
15 node to said ground.

1 13. (Original) The method according to Claim 12 wherein said optimal
2 capacitance value is calculated using a formula based on capacitance loading in
3 switching circuits and capacitance loading in non-switching circuits.

1 14. (Original) The method according to Claim 12 wherein said operating mode
2 comprises a power-saving mode.

1 15. (Original) The method according to Claim 12 wherein said capacitor
2 comprises an MOS device.

1 16. (Original) The method according to Claim 12 wherein said capacitor is
2 connected to said upper voltage node and said switch is connected to said ground.

1 17. (Original) The method according to Claim 12 wherein said capacitor is
2 connected to said ground and said switch is connected to said upper voltage node.

1 18. (Original) The method according to Claim 12 wherein said switch comprises
2 an MOS transistor.

1 19. (Amended) An integrated circuit device comprising:
2 an upper voltage node;
3 a ground;
4 a plurality of switchable capacitors wherein each said switchable capacitor is
5 connected from said upper voltage node to said ground;
6 [a] means for [of] tracking the operating mode of said integrated circuit device;
7 [a] means for [of] selecting an optimal capacitance value based on said operating
8 mode; and
9 [a] means for [of] selecting a set of said switchable capacitors from said plurality
10 of switchable capacitors to thereby connect said optimal capacitance value from said
11 upper voltage node to said ground.

1 20. (Amended) The device according to Claim 19 wherein said means of selecting
2 an optimal capacitance value based on said operating mode comprises:
3 [a] means for [of] determining a proportion of total circuits in said integrated
4 circuit device that are switching in said operating mode; and
5 [a] means for [of] calculating said optimal capacitance value based on said
6 proportion.

1 21. (Original) The device according to Claim 20 wherein said optimal capacitance
2 value is calculated using a formula based on capacitance loading in switching circuits
3 and capacitance loading in non-switching circuits.

1 22. (Original) The device according to Claim 19 wherein said operating mode
2 comprises a power-saving mode.

1 23. (Original) The device according to Claim 19 wherein said switchable
2 capacitors each comprise a capacitor and a switch connected in series.

1 24. (Original) The device according to Claim 23 wherein said capacitor comprises
2 an MOS device.

1 25. (Original) The device according to Claim 23 wherein said capacitor is
2 connected to said upper voltage node and said switch is connected to said ground.

1 26. (Original) The device according to Claim 23 wherein said capacitor is
2 connected to said ground and said switch is connected to said upper voltage node.

1 27. (Original) The device according to Claim 23 wherein said switch comprises
2 an MOS transistor.

1 28. (Original) The device according to Claim 19 wherein said switchable
2 capacitors each comprise:

3 a PMOS transistor having source, drain, and gate terminals wherein said source
4 terminal is coupled to said upper voltage node;

5 an NMOS transistor having source, drain, and gate terminals wherein said
6 source terminal is coupled to said ground, wherein said drain terminal is coupled to said
7 PMOS transistor gate terminal, and wherein said gate terminal is coupled to said PMOS
8 transistor drain terminal;

9 a first switch coupled between said PMOS transistor gate terminal and said
10 upper voltage node; and

11 a second switch coupled between said NMOS transistor gate terminal and said
12 ground.

1 29. (Original) The device according to Claim 28 wherein said first and second
2 switches comprise MOS transistors.

1 30. (Original) The device according to Claim 28 wherein said first and second
2 switches are controlled by a single signal.

1 31. (Newly Added) A method to reduce switching noise on an integrated circuit
2 device, said method comprising:

3 providing an integrated circuit device comprising an upper voltage node, a
4 ground, and a plurality of switchable capacitors wherein each said switchable capacitor
5 is connected from said upper voltage node to said ground;

6 tracking an operating mode of said integrated circuit device;

7 selecting an optimal capacitance value based on said operating mode by
8 determining a proportion of total circuits in said integrated circuit device that are
9 switching in said operating mode and calculating said optimal capacitance value based
10 on said proportion; and

11 selecting a set of said switchable capacitors from said plurality of switchable
12 capacitors to thereby connect said optimal capacitance value from said upper voltage
13 node to said ground.

1 32. (Newly Added) An integrated circuit device comprising:

2 an upper voltage node;

3 a ground;

4 a plurality of switchable capacitors wherein each said switchable capacitor is
5 connected from said upper voltage node to said ground;

6 means for tracking the operating mode of said integrated circuit device;

7 means for selecting an optimal capacitance value based on said operating mode;

8 and

9 means for selecting a set of said switchable capacitors from said plurality of
10 switchable capacitors to thereby connect said optimal capacitance value from said

- 11 upper voltage node to said ground, wherein said means of selecting an optimal
12 capacitance value based on said operating mode comprises:
13 means for determining a proportion of total circuits in said integrated circuit
14 device that are switching in said operating mode; and
15 means for calculating said optimal capacitance value based on said proportion.